ERICSSON

February 1999

PBM 3960/1
Microstepping Controller/ Dual Digital-to-Analog Converter

Description

PBM 3960/1 is a dual 7-bit+sign, Digital-to-Analog Converter (DAC) especially developed to be used together with the PBL 3771/1, Precision Stepper Motor driver in micro-stepping applications. The circuit has a set of input registers connected to an 8-bit data port for easy interfacing directly to a microprocessor. Two registers are used to store the data for each seven-bit DAC, the eighth bit being a sign bit (sign/ magnitude coding). A second set of registers are used for automatic fast/slow current decay control in conjunction with the PBL 3771/1, a feature that greatly improves high-speed micro-stepping performance. The PBM 3960/1 is fabricated in a high-speed CMOS process.

Key Features

- Analog control voltages from 3 V down to 0.0 V.
- High-speed microprocessor interface.
- Automatic fast/slow current decay control.
- Full-scale error ±1 LSB.
- Interfaces directly with TTL levels and CMOS devices.
- Fast conversion speed, 3 µs.
- Matches PBL 3771.

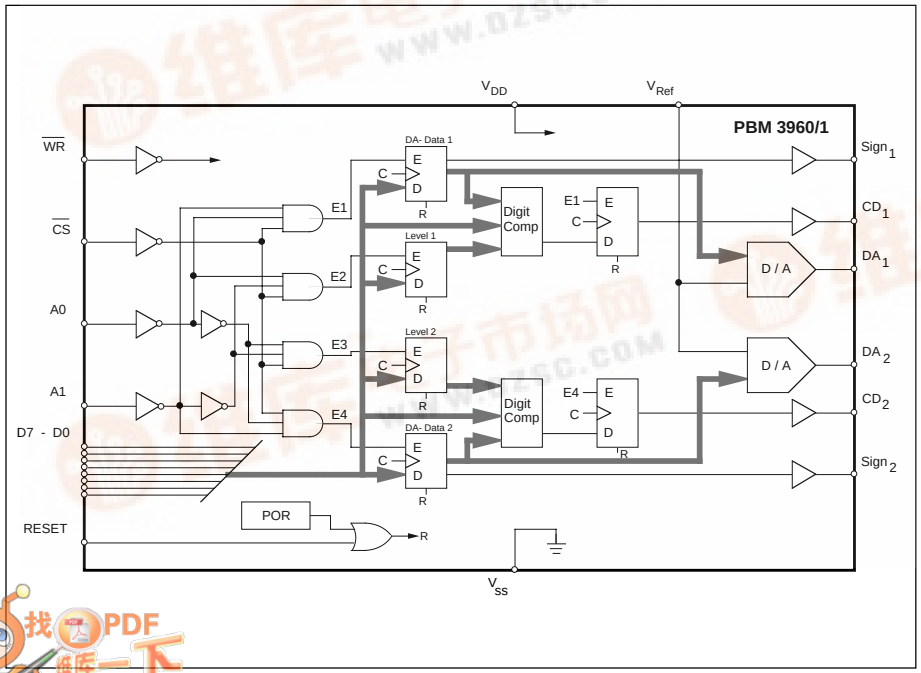
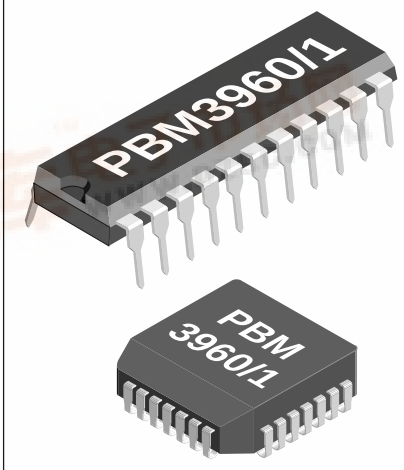


Figure 1. Block Diagram.



22-pin plastic DIP
28-pin plastic PLCC

Maximum Ratings

Parameter	Pin no. *	Symbol	Min	Max	Unit
Voltage					
Supply	5	V_{DD}		6	V
Logic inputs	6- 17	V_I	-0.3	V_{DD}+ 0.3	V
Reference input	1	V_R	-0.3	V_{DD}+ 0.3	V
Current					
Logic inputs	6- 17	I_I	-0.4	+0.4	mA
Temperature					
Storage temperature		T_S	-55	+150	°C
Operating ambient temperature		T_J	-20	+85	°C

* refers to DIP package

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	4.75	5.0	5.25	V
Reference voltage	V_R	0	2.5	3.0	V

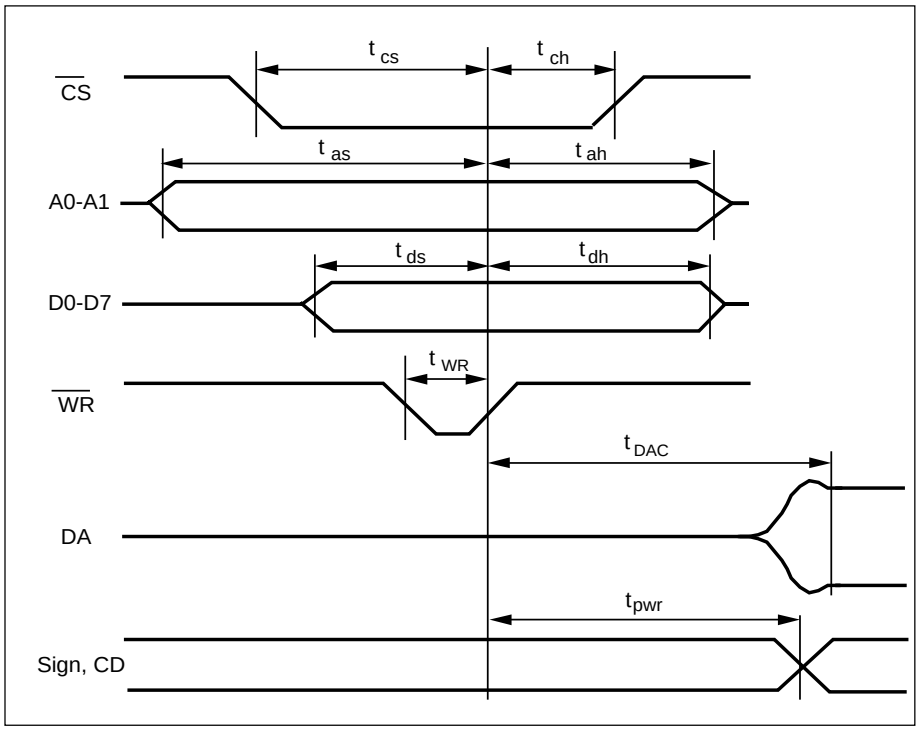


Figure 2. Timing.

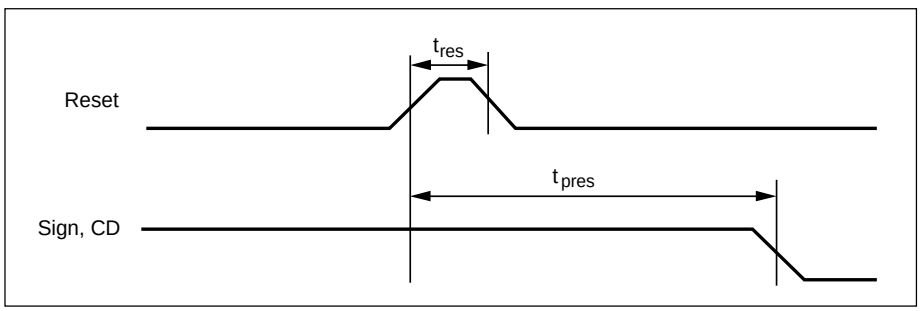


Figure 3. Timing of Reset.

Electrical Characteristics

Electrical characteristics over recommended operating conditions.

Parameter	Symbol	Ref. fig	Conditions	Min	Typ	Max	Unit
Logic Inputs							
Reset logic HIGH input voltage	V_{IHR}			3.5			V
Reset logic LOW input voltage	V_{ILR}					0.1	V
Logic HIGH input voltage	V_{IH}			2.0			V
Logic LOW input voltage	V_{IL}					0.8	V
Reset input current	I_{IR}		$V_{SS} < V_{IR} < V_{DD}$	-0.01		1	mA
Input current, other inputs	I_I		$V_{SS} < V_I < V_{DD}$	-1		1	µA
Input capacitance					3		pF
Internal Timing Characteristics							
Address setup time	t_{as}	2	Valid for A0, A1	60			ns
Data setup time	t_{ds}	2	Valid for D0 - D7	60			ns
Chip select setup time	t_{cs}	2		70			ns
Address hold time	t_{ah}	2				0	ns
Data hold time	t_{dh}	2				0	ns
Chip select hold time	t_{ch}	2				0	ns
Write cycle length	t_{WR}	2		50			ns
Reset cycle lenght	t_R	3		80			ns
Reference Input							
Input resistance	R_{Ref}			6	9		kΩ
Logic Outputs							
Logic HIGH output current	I_{OH}		V_O = 2.4 V		-13	-5	mA
Logic LOW output current	I_{OL}		V_O = 0.4 V	1.7	5		mA
Write propagation delay	$t_{p_{WR}}$	2	From positive edge of WR. outputs valid, C_{load} = 120 pF		30	100	ns
Reset propagation delay	t_{p_R}	3	From positive edge of Reset to outputs valid, C_{load} = 120 pF		60	150	ns
DAC Outputs			Reset open, V_{Ref} = 2.5 V				
Nominal output voltage	V_{DA}			0		V_{Ref} - 1LSB	V
Resolution					7		Bits
Offset error		7			0.2	0.5	LSB
Gain error		7			0.1	0.5	LSB
Endpoint nonlinearity		7			0.2	0.5	LSB
Differential nonlinearity		5, 6			0.2	0.5	LSB
Load error			(V_{DA}, unloaded - V_{DA}, loaded) R_{load} = 2.5 kΩ, Code 127 to DAC		0.1	0.5	LSB
Power supply sensitivity			Code 127 to DAC 4.75 V < V_{DD} < 5.25 V		0.1	0.3	LSB
Conversion speed	t_{DAC}	2	For a full-scale transition to ±0.5 LSB of final value, R_{load} = 2.5 kohm, C_{load} = 50 pF.		3	8	µs

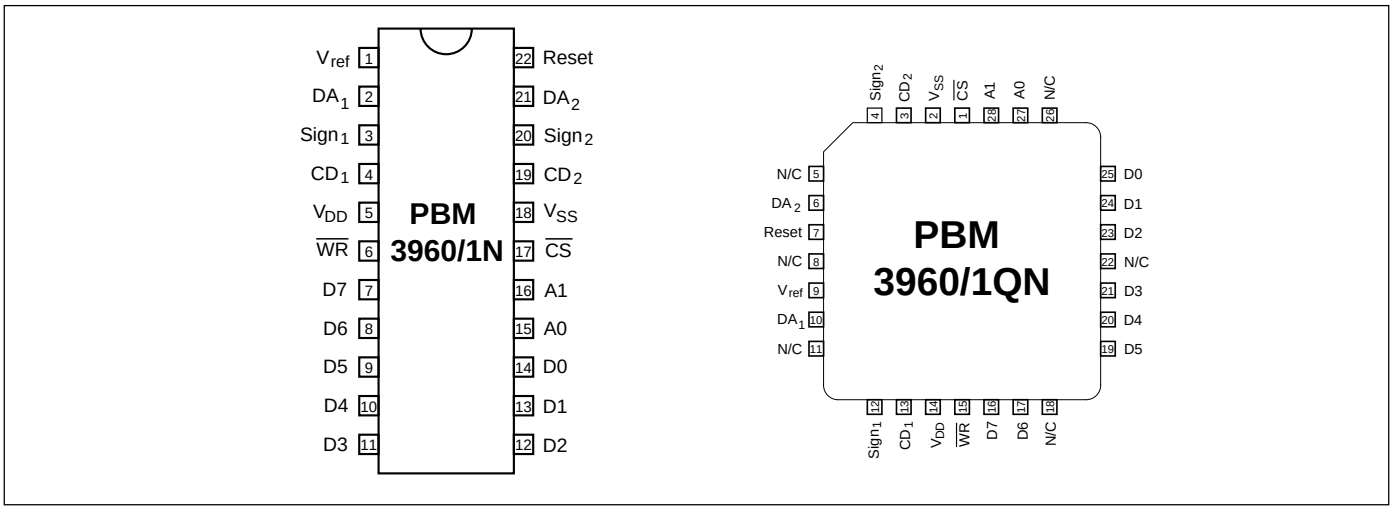


Figure 4. Pin configuration.

Pin Descriptions

Refer to figure 4.

DIP	PLCC	Symbol	Description
1	9	V_{Ref}	Voltage reference supply pin, 2.5 V nominal (3.0 V maximum)
2	10	DA_1	Digital-to-Analog 1, voltage output. Output between 0.0 V and V_R - 1 LSB.
3	12	$Sign_1$	Sign 1, TTL/CMOS level. To be connected directly to PBL 3771 Phase input. Databit D7 is transfered non inverted from PBM 3960/1/1 data input.
4	13	CD_1	Current Decay 1, TTL/CMOS level. The signal is automatically generated when decay level is programmed. LOW level = fast current decay.
5	14	V_{DD}	Voltage Drain-Drain, logic supply voltage. Normally +5 V.
6	15	$\overline{WR}$	Write, TTL/CMOS level, input for writing to internal registers. Data is clocked into flip flops on positive edge.
7	16	D7	Data 7, TTL/CMOS level, input to set data bit 7 in data word.
8	17	D6	Data 6, TTL/CMOS level, input to set data bit 6 in data word.
9	19	D5	Data 5, TTL/CMOS level, input to set data bit 5 in data word.
10	20	D4	Data 4, TTL/CMOS level, input to set data bit 4 in data word.
11	21	D3	Data 3, TTL/CMOS level, input to set data bit 3 in data word.
12	23	D2	Data 2, TTL/CMOS level, input to set data bit 2 in data word.
13	24	D1	Data 1, TTL/CMOS level, input to set data bit 1 in data word.
14	25	D0	Data 0, TTL/CMOS level, input to set data bit 0 in data word.
15	27	A0	Address 0, TTL/CMOS level, input to select data transfer, A0 selects between cannel 1 (A0 = LOW) and channel 2 (A0 = HIGH).
16	28	A1	Address 1, TTL/CMOS level, input to select data transfer. A1 selects between normal D/A register programming (A1 = LOW) and decay level register programming (A1 = HIGH).
17	1	$\overline{CS}$	Chip Select, TTL/CMOS level, input to select chip and activate data transfer from data inputs. LOW level = chip is selected.
18	2	V_{SS}	Voltage Source-Source. Ground pin, 0 V reference for all signals and measurements unless otherwise noted.
19	3	CD_2	Current Decay 2, TTL/CMOS level. The signal is automatically generated when decay level is programmed. LOW level = fast current decay .
20	4	$Sign_2$	Sign 2. TTL/CMOS level. To be connected directly to PBL 3771 sign input. Data bit D7 is transfered non-inverted from PBM 3960/1 data input.
21	6	DA_2	Digital-to-Analog 2, voltage output. Output between 0.0 V and V_{ref} - 1 LSB.
22	7	Reset	Reset, digital input resetting internal registers. HIGH level = Reset, $V_{Res} \geq 3.5$ V = HIGH level. Pulled low internally.
	5		Not Connected
	8		Not Connected
	11		Not Connected
	18		Not Connected
	22		Not Connected
	26		Not Connected

Definition of Terms

Resolution

Resolution is defined as the reciprocal of the number of discrete steps in the DAC output. It is directly related to the number of switches or bits within the DAC. For example, PBM 3960/1 has 2^7, or 128, output levels and therefor has 7 bits resolution. Remember that this is not equal to the number of microsteps available.

Linearity Error

Linearity error is the maximum deviation from a straight line passing through the end points of the DAC transfer characteristic. It is measured after adjusting for zero and full scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

Power Supply Sensitivity

Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

Settling Time

Full-scale current settling time requires zero-to-full-scale or full-scale-to-zero output change. Settling time is the time required from a code transition until the DAC output reaches within $\pm^1/_2$LSB of the final output value.

Full-scale Error

Full-scale error is a measure of the output error between an ideal DAC and the actual device output.

Differential Non-linearity

The difference between any two consecutive codes in the transfer curve from the theoretical 1LSB, is differential non-linearity

Monotonic

If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. A 7-bit DAC which is monotonic to 7 bits simply means that increasing digital input codes will produce an increasing analog output. PBM 3960/1 is monotonic to 7 bits.

Functional Description

Each DAC channel contains two registers, a digital comparator, a flip flop, and a D/A converter. A block diagram is shown on the first page. One of the registers stores the current level, below which, fast current decay is initiated. The status of the CD outputs determines a fast or slow current decay to be used in the driver.

The digital comparator compares each new value with the previous one and the value for the preset level for fast current decay. If the new value is strictly lower than both of the others, a fast current decay condition exists. The flip flop sets the CD output. The CD output is updated each time a new value is loaded into the D/A register. The fast current decay signals are used by the driver circuit, PBL 3771/1, to change the current control scheme of the output stages. This is to avoid motor current dragging which occurs at high stepping rates and during the negative current slopes, as illustrated in figure 9. Eight different levels for initiation of fast current decay can be selected.

The sign outputs generate the phase shifts, i.e., they reverse the current direction in the phase windings.

Data Bus Interface

PBM 3960/1 is designed to be compatible with 8-bit microprocessors such as the 6800, 6801, 6803, 6808, 6809, 8051, 8085, Z80 and other popular types and their 16/32 bit counter parts in 8 bit data mode. The data bus interface consists of 8 data bits, write signal, chip select, and two address pins. All inputs are TTL-compatible (except reset). The two address pins control data transfer to the four internal D-type registers. Data is transferred according to figure 10 and on the positive edge of the write signal.

Current Direction, $Sign_1$ & $Sign_2$

These bits are transferred from D_7 when writing in the respective DA register. A_0 and A_1 must be set according to the data transfer table in figure 10.

Current Decay, CD_1 & CD_2

CD_1 and CD_2 are two active low signals (LOW = fast current decay). CD_1 is active if the previous value of DA-Data1 is strictly larger than the new value of DA-Data1 and the value of the level register LEVEL1 (L_{61} … L_{41}) is strictly larger than the new value of DA-Data1. CD_1 is updated every time a new value is loaded into DA-Data1. The logic definition of CD_1 is:

$$CD_1 = \text{NOT}\{[(D_6 \ldots D_0) < (Q_{61} \ldots Q_{01})] \text{ AND } [(D_6 \ldots D_4) < (L_{61} \ldots L_{41})]\}$$

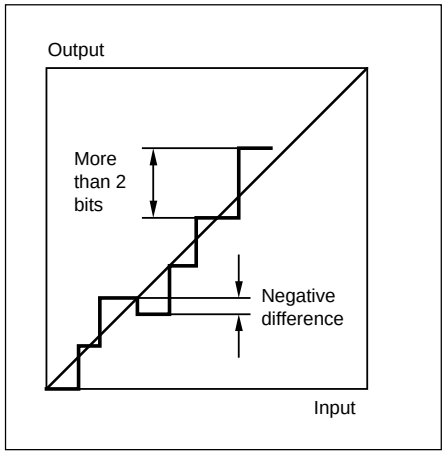


Figure 5. Errors in D/A conversion. Differential non-linearity of more than 1 bit, output is non-monotonic.

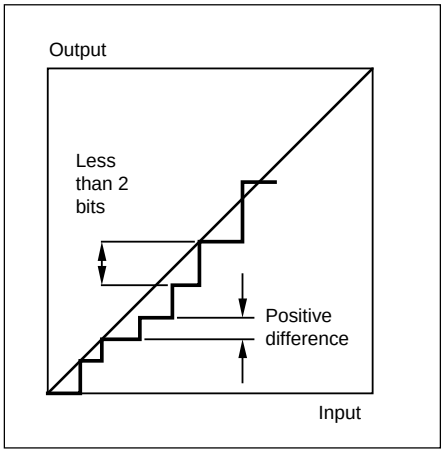


Figure 6. Errors in D/A conversion. Differential non-linearity of less than 1 bit, output is monotonic.

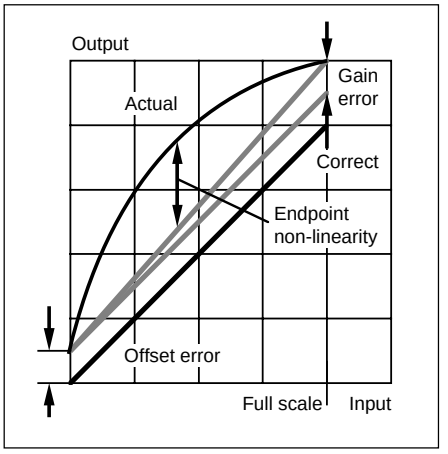


Figure 7. Errors in D/A conversion. Non-linearity, gain and offset errors.

Where (D_6 … D_0) is the new value being sent to DA-Data1 and (Q_{61} … Q_{01}) is DA-Data1's old value. (L_{61} … L_{41}) are the three bits for setting the current decay level at LEVEL1.

The logic definition of CD_2 is analog to CD_1:

CD_2 = NOT{[(D_6 … D_0) < (Q_{62} … Q_{02})] AND[(D_6 …D_4) < (L_{62} … L_{42})]}

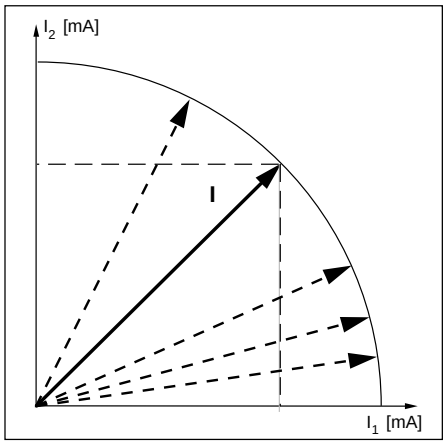


Figure 8a. Assuming that torque is proportional to the current in resp. winding it is possible to draw figure 8b.

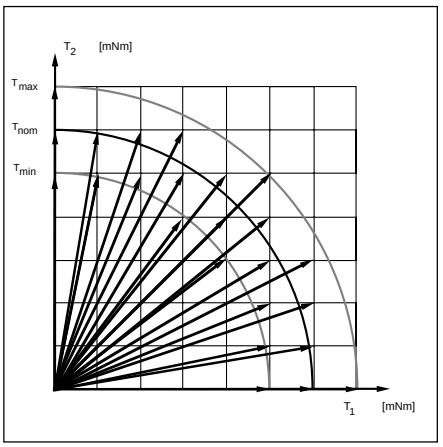


Figure 8b. An example of accessible positions with a given torque deviation/ fullstep. Note that 1:st µstep sets highest resolution. Data points are exaggerated for illustration purpose.
TNom = code 127.

Where (L_{62} … L_{42}) is the level programmed in channel 2's level register. (D_6 … D_0) and (Q_{62} … Q_{02}) are the new and old values of DA-Data2.

The two level registers, LEVEL1 and LEVEL2, consist of three flip flops each and they are compared against the three most significant bits of the DA-Data value, sign bit excluded.

DA_1 and DA_2

These are the two outputs of DAC1 and DAC2. Input to the DACs are internal data bus (Q_{61} … Q_{01}) and (Q_{62} … Q_{02}).

Reference Voltage V_{Ref}

V_{Ref} is the analog input for the two DACs. Special care in layout, gives a very low voltage drop from pin to resistor. Any V_{Ref} between 0.0 V and V_{DD} can be applied, but output might be non-linear above 3.0 V.

Power-on Reset

This function automatically resets all internal flip flops at power-on. This results in V_{SS} voltage at both DAC outputs and all digital outputs.

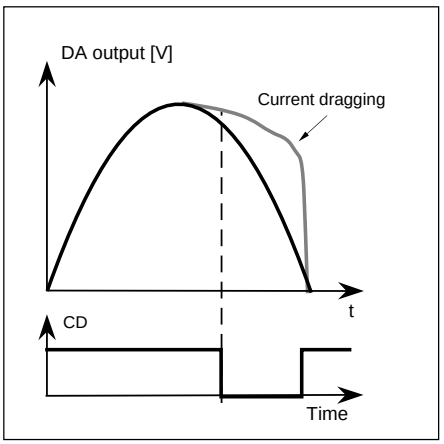


Figure 9. Motor current dragging at high step rates and current decay influence. Fast current decay will make it possible for the current to follow the ideal sine curve. Output shown without sign shift.

$\overline{CS}$	A0	A1	Data Transfer
0	0	0	D7 —> Sign1, (D6—D0) —> (Q61—Q01), New value —> CD1
0	0	1	(D6—D4) —> (L61—L41)
0	1	0	D7 —> Sign2, (D6—D0) —> (Q62—Q02), New value —> CD2
0	1	1	(D6—D4) —> (L62—L42)
1	X	X	No Transfer

Figure 10. Table showing how data is transfered inside PBM 3960/1.

Reset

If Reset is not used, leave it disconnected. Reset can be used to measure leakage currents from V_{DD}.

Applications Information

How Many Microsteps?

The number of true microsteps that can be obtained depends upon many different variables, such as the number of data bits in the Digital-to-Analog converter, errors in the converter, acceptable torque ripple, single- or double-pulse programming, the motor's electrical, mechanical and magnetic characteristics, etc. Many limits can be found in the motor's ability to perform properly; overcome friction, repeatability, torque linearity, etc. It is important to realize that the number of current levels, 128 (2^7), is *not* the number of steps available. 128 is the number of current levels (reference voltage levels) available from each driver stage. Combining a current level in one winding with any of 128 other current levels in the other winding will make up 128 current levels. So expanding this, it is possible to get 16,384 (128 • 128) combinations of different current levels in the two windings. Remember that these 16,384 micro-positions are not all useful, the torque will vary from 100% to 0% and some of the options will make up the same position. For instance, if the current level in one winding is OFF (0%) you can still vary the current in the other winding in 128 levels. All of these combinations will give you the same position *but* a varying torque.

Typical Application

The microstepper solution can be used in a system with or without a microprocessor.
Without a microprocessor, a counter addresses a ROM where appropriate step data is stored. Step and Direction are the input signals which represent clock and up / down of counter. This is the ideal solution for a system where there is no microprocessor or it is heavily loaded with other tasks.
With a microprocessor, data is stored in ROM / RAM area or each step is successively calculated. PBM 3960/1 is connected like any peripheral addressable device. All parts of stepping can be tailored for specific damping needs etc.

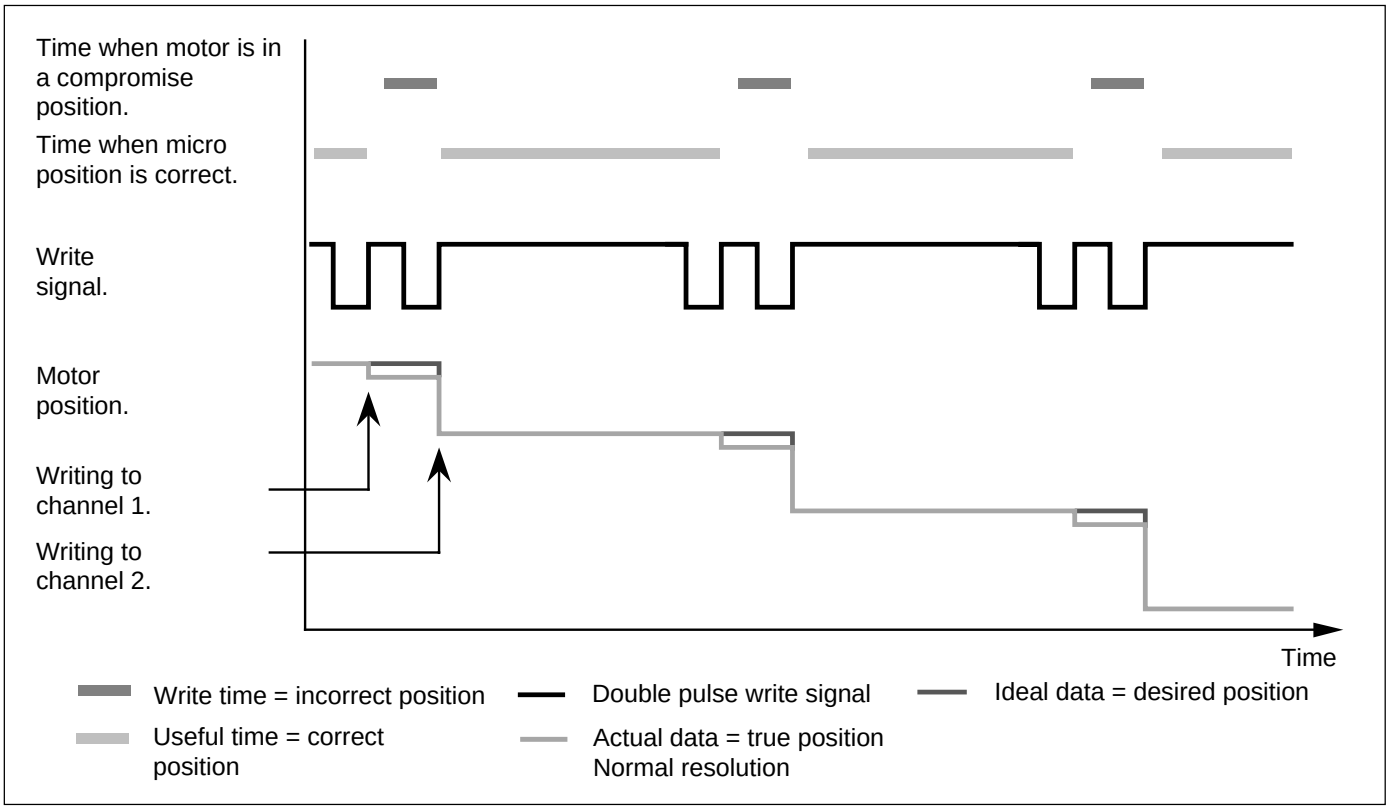


Figure 11. Double pulse programming, in- and output signals.

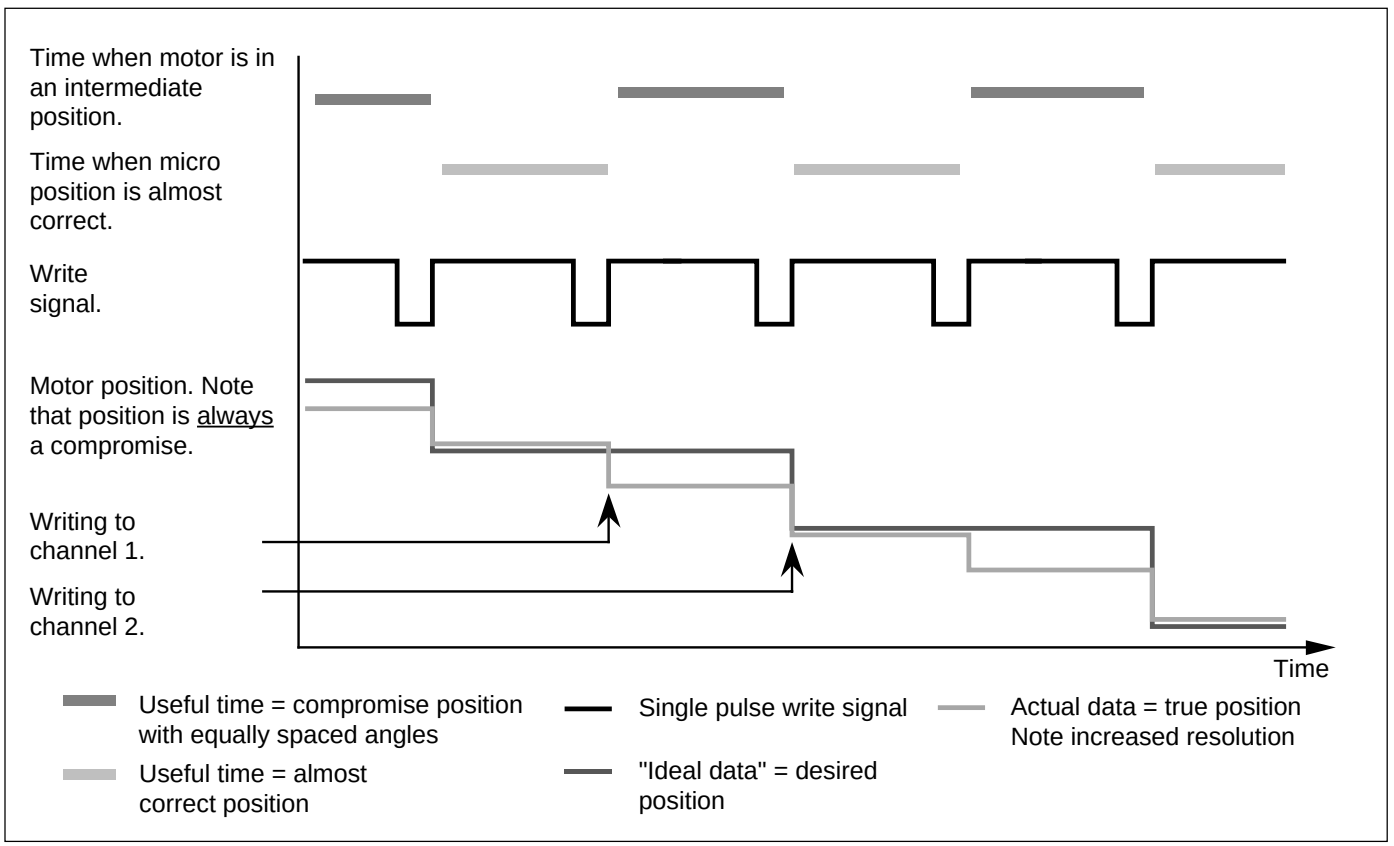


Figure 12. Single pulse programming, in- and output signals.

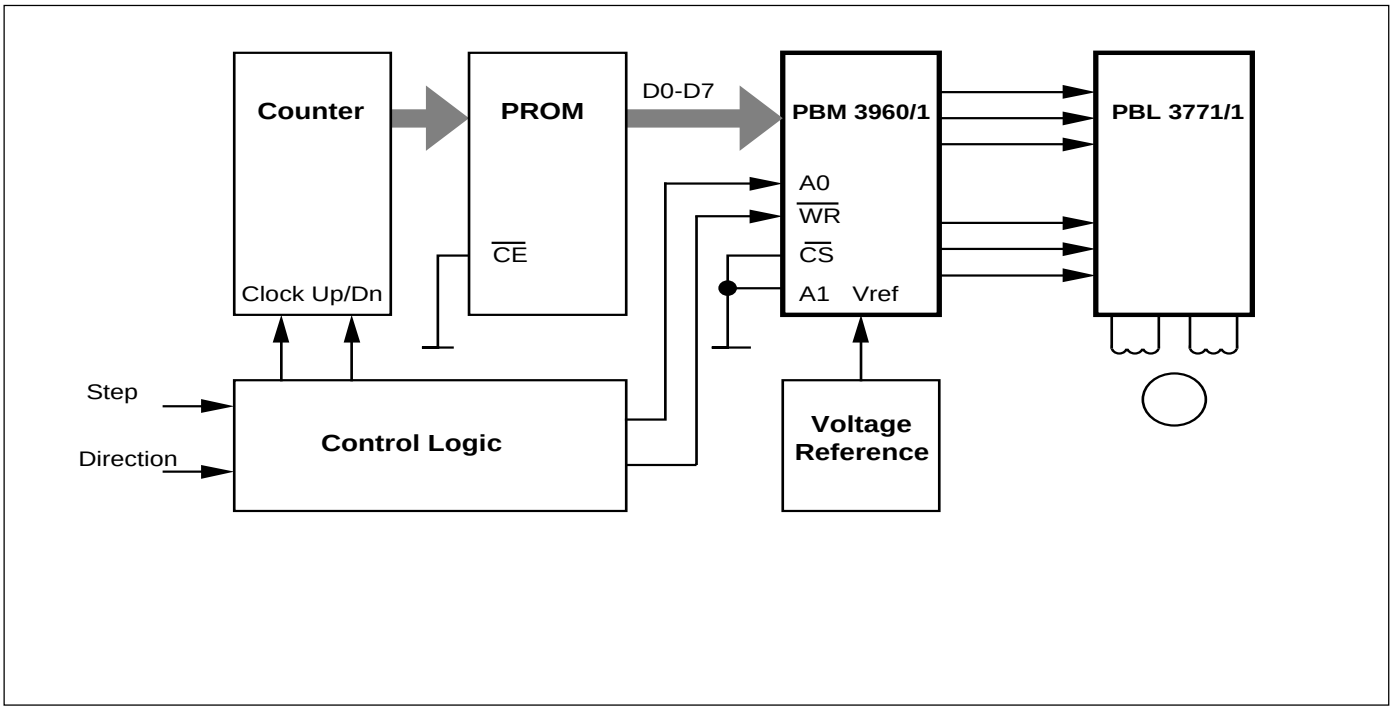


Figure 13. Typical blockdiagram of an application without a microprocessor. Available as testboard, TB 307i/2.

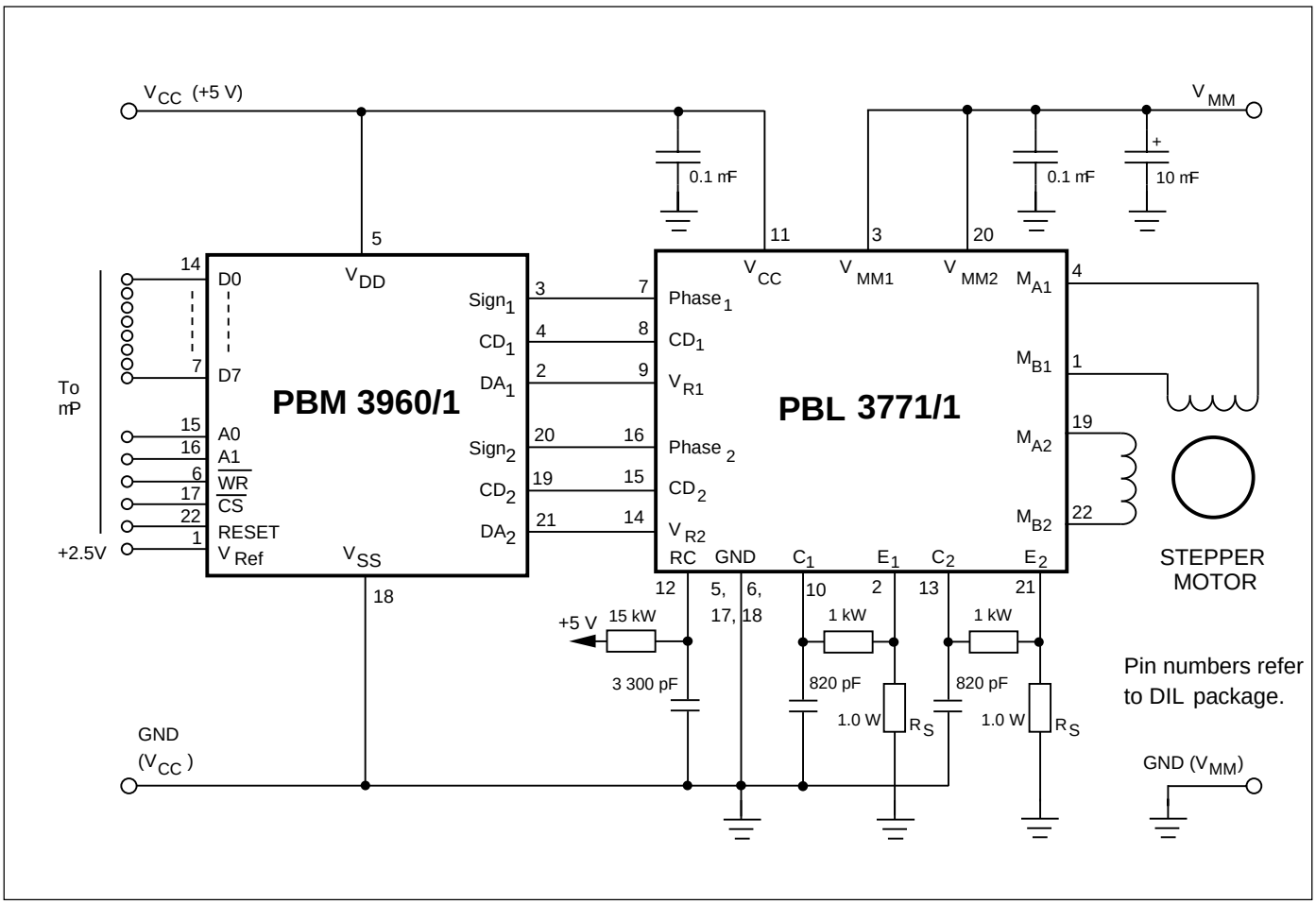


Figure 14. Typical application in a microprocessor based system.

This is the ideal solution for a system where there is an available microprocessor with extra capacity and low cost is more essential than simplicity. See typical application, figure 14.

User Hints

Never disconnect ICs or PC Boards when power is supplied.

Choose a motor that is rated for the current you need to establish desired torque. A high supply voltage will gain better stepping performance even if the motor is not rated for the V_{MM} voltage, the current regulation in PBL 3771/1 will take care of it. A normal stepper motor might give satisfactory result, but while microstepping, a “microstepping-adapted” motor is recommended. This type of motor has smoother motion due to two major differences, the stator / rotor teeth relationship is non-equal and the static torque is lower.

The PBM 3960/1 can handle programs which generate microsteps at a desired resolution as well as quarter stepping, half stepping, full stepping, and wave drive.

Fast or Slow Current Decay?

There is a difference between static and dynamic operation of which the actual application must decide upon when to use fast or slow current decay. Generally slow decay is used when stepping at slow speeds. This will give the benefits of low current ripple in the drive stage, a precise and high overall average current, and normal current increase on the positive edge of the sine-cosine curves. Fast current decay is used at higher speeds to avoid current dragging with lost positions and incorrect step angles as a result.

Ramping

Every drive system has inertia which must be considered in the drive system. The rotor and load inertia play a big role at higher speeds. Unlike the DC motor, the stepper motor is a synchronous motor and does not change its speed due to load variations. Examining a typical stepper motor’s torque-versus-speed curve indicates a sharp torque drop-off for the “start-stop without error” curve. The reason for this is that the torque requirements increase by the cube of the speed change. For good motor performance, controlled acceleration and deceleration should be considered even though microstepping will improve overall performance.

Programming PBM 3960/1

There are basically two different ways of programming the PBM 3960/1. They are called “single-pulse programming” and “double-pulse programming.” Writing to the device can only be accomplished by addressing one register at a time. When taking one step, at least two registers are normally updated. Accordingly there must be a certain time delay between writing to the first and the second register. This programming necessity gives some special stepping advantages.

Double-pulse Programming

The normal way is to send two write pulses to the device, with the correct addressing in between, keeping the delay between the pulses as short as possible. Write signals will look as illustrated in figure12. The advantages are:

- low torque ripple
- correct step angles between each set of double pulses
- short compromise position between the two step pulses
- normal microstep resolution

Single-pulse Programming

A different approach is to send one pulse at a time with an equally-spaced duty cycle. This can easily be accomplished and any two adjacent data will make up a microstep position. Write signals will look as in figure 13. The advantages are:

- higher microstep resolution
- smoother motion

The disadvantages are:

- higher torque ripple
- compromise positions with almost-correct step angles

ERICSSON

Ordering Information

Package	Part No.
DIP Tube	PBM 3960/1NS
PLCC Tube	PBM 3960/1QNS
PLCC Tape & Reel	PBM 3960/1QNT

Specifications subject to change without notice.

1522-PBM 3960/1 Uen Rev. B

ERICSSON

Ericsson Components AB
SE-164 81 Kista-Stockholm, Sweden
Telephone: +46 8 757 50 00